REMARKS

Claims 1-81 are pending. Claims 28-81 have been withdrawn from examination pending allowance of a generic claim as provided in 37 CFR 1.141.

Section 102(b) Rejections

Reconsideration is requested of the rejection of claims 1-8 and 17-18 under 35 U.S.C. §102(b) as being anticipated by Takada et al. (5,855,735).

Claim 1 is directed to a process for re-use of a silicon wafer having, *inter alia*, a precipitate free zone having a thickness of at least 20 μm adjacent the front surface. As used in claim 1 and is generally understood in the context of silicon wafers, a "precipitate free zone" is understood to mean a zone having an absence of **oxygen** precipitates.[1] In the process of claim 1, the wafer is subjected to an oxide growth step to form an oxide layer having a thickness of at least 2 nm, the oxidized wafer is thinned to provide a thinned wafer having a thinned precipitate free zone, and polishing the front surface of the thinned wafer to a specular surface.

Takada et al. also disclose a process for re-use of a silicon wafer. In their process, Takada et al. induce microfractures in the surface using a rotating pad and abrasive slurry until the surface layer materials are removed, and chemically etch the resulting wafer until the microfractures are removed. Takada et al., however, do not disclose whether their starting wafer has a precipitate free zone ***of any thickness*** and there is no basis for concluding that such zones ***of any thickness*** would invariably be present in Takada et al.'s starting wafers. It necessarily follows, therefore, that Takada et al. do not disclose or suggest a process for re-use of a silicon wafer having a precipitate free zone with a thickness at least 20 μm adjacent the front surface.

Takada et al. also fail to disclose subjecting a wafer to be re-used to an oxide growth step to form an oxide layer having a thickness of at least 2 nm and thinning the oxidized wafer. At column 2, lines 25-35, Takada et al. merely disclose that oxide films

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[1]See applicant's specification at p. 6, line 1-13.

may be one of the myriad "foreign materials" that their process may be used to remove. Takada et al. do not affirmatively disclose or suggest oxidizing the wafer as part of the reclamation process.

Finally, Takada et al. fail to disclose or suggest thinning the wafer in a manner to yield a thinned wafer having **a thinned precipitate free zone**. Stated another way, Takada et al. do not disclose or suggest controlling the thinning process in a manner which leaves a precipitate free zone adjacent the surface of the wafer. At column 2, line 40 to column 3, line 12, Takada et al. merely discuss the known material-removal technique of lapping. Lapping a wafer and removing any resulting damage is, in no respect, equivalent to forming a precipitate free zone or leaving a precipitate free zone of any thickness.

As stated in M.P.E.P. § 2131, a claim is anticipated only if each and every element of the claim is found in a single prior art reference. Takada et al. do not meet this standard because they fail to disclose using a wafer having a precipitate free zone ***of any thickness***, oxidizing this wafer, thinning the oxidized wafer to yield a wafer having a thinned precipitate free zone, and polishing the thinned wafer. As such, Takada et al. do not anticipate claim 1.

Each of claims 2-8, 17 and 18 depend, directly or indirectly, from claim 1 and thus, are not anticipated by Takada et al. for the same reasons as those stated with respect to claim 1. In addition, these claims introduce further requirements which are similarly lacking in Takada et al.'s disclosure. For example, claims 6 and 8 require that the polished and thinned wafer be *at least* 30 μm thinner than the wafer was prior to the oxide growth stage, *i.e.*, that the total wafer thickness reduction be at least 30 μm. In contrast, Takada et al. disclose that the total wafer thickness reduction be "no greater than 30 microns." (Col. 5, line 39-40, see also Table 1). As such, Takada et al. fail to disclose any process where the thinned and polished wafer is at least 30 μm thinner than before any re-use processing stage.

Section 103 Rejections:

Reconsideration is requested of the rejection of claims 9-16 and 19-24 under 35 U.S.C. §103(a) as being unpatentable over Takada et al. (5,855,735) in view of Mule'Stagno et al. (6,284,039).

Claims 9-16 and 19-24 depend, directly or indirectly, from claim 1 and are distinguishable from Takada et al. for the reasons noted above in connection with claim 1. Mule'Stagno et al. (6,284,039) add nothing to Takada et al's disclosure which renders the invention defined by these claims obvious.

Mule'Stagno et al. are primarily concerned with the avoidance of the formation of agglomerated intrinsic point defects, *i.e.*, the agglomeration of crystal lattice vacancies and silicon self-interstitial atoms. Significantly, intrinsic point defects (*i.e.*, crystal lattice vacancies and silicon self-interstitial atoms)[2] and agglomerated intrinsic point defects (*i.e.*, the types of defects which form as the result of an agglomeration of crystal lattice vacancies or silicon self-interstitial atoms such as D-defects, Flow Pattern defects, oxygen induced stacking fault nuclei and interstitial-type dislocation loops)[3] are distinguishable from oxygen precipitates. Secondarily, Mule'Stagno et al. are concerned with the avoidance of enhanced oxygen clustering which may occur in silicon in which vacancies are the predominant intrinsic point. According to Mule'Stagno et al., enhanced oxygen precipitation may occur in this region depending upon the concentration of oxygen in the silicon and thermal history of the silicon; to avoid this effect, they suggest starting with low oxygen content silicon or thermally annealing the silicon to dissolve any oxygen clusters formed during crystal pulling which may later be grown into oxygen precipitates.[4] Furthermore, Mule'Stagno et al. describe and illustrate

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[2]Mule'Stagno et al., U.S. Patent No. 6,284,039 at column 1, lines 42-43.

[3]Mule'Stagno et al., U.S. Patent No. 6,284,039 at column 1, line 44 - column 2, line 7.

[4]Mule'Stagno et al., U.S. Patent No. 6,284,039 at column 11, line 30 - column 12, line 26.

(in Fig. 5) the relative position of vacancy and interstitial dominated regions; in general, vacancy dominated regions occur radially inward of interstitial dominated regions; to the extent Mule'Stagno et al. discuss the avoidance of oxygen precipitation, therefore, they discuss it in the context of an axially symmetric region (*e.g.*, an annulus about the axis of an ingot or wafer). In contrast, claim 1 is directed to a precipitate free zone adjacent the front surface as illustrated in Fig. 3 (element 37).

Mule'Stagno et al. do not disclose or address, in any respect, any advantages which may be derived by re-use of a silicon wafer from an aborted integrated circuit device fabrication process. Nor do they disclose the formation of precipitate free zones, of any thickness, in a region adjacent the front surface of the wafer. It necessarily follows, therefore, that Mule'Stagno et al. do not suggest processing, for re-use, a wafer having a precipitate free zone of at least 20 micrometers, oxidizing the surface of the wafer, thinning the oxidized wafer to produce a wafer having a thinned precipitate free zone, and polishing the thinned wafer.

Whether viewed individually or in combination, Takada et al. and Mule'Stagno et al. fail to disclose any step of the process defined by claim 1 and the claims which depend therefrom. Neither Takada et al. nor Mule'Stagno et al. disclose oxidizing a wafer having a precipitate free zone of at least 20 micrometers. Neither Takada et al. nor Mule'Stagno et al. disclose thinning such a wafer to form a wafer having a thinned precipitate free zone. Neither Takada et al. nor Mule'Stagno et al. disclose polishing a wafer having a thinned precipitate free zone. It necessarily follows, therefore, that claims 9-16 and 19-24 which depend from claim 1 are patentable over the combined disclosures of these two references.

Reconsideration is requested of the rejection of claims 25-27 under 35 U.S.C. 103(a) in view of Takada et al. As pointed out previously, Takada et al. fail to disclose forming an oxide layer of ***any*** thickness for ***any*** reason on a wafer having a precipitate free zone of ***any*** thickness. As a result, a person of ordinary skill would not have been motivated by Takada et al. to grow an oxide layer having a thickness as specified in any of claims 25-27 on a wafer having a precipitate free zone of a thickness of at least 20

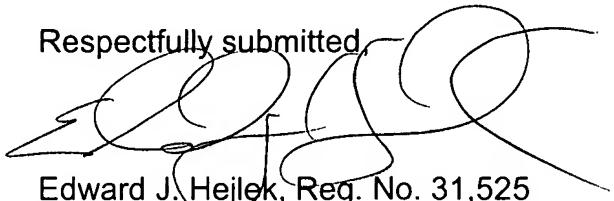
micrometers and then thinning the oxidized wafer to yield a thinned precipitate free zone and polishing the thinned wafer.

In view of the foregoing, applicant respectfully requests that the Examiner issue a Notice of Allowance for claims 1-27. In addition, the remaining claims, *i.e.*, claims 28-81 may now be rejoined and examined in accordance with 37 CFR 1.141.

CONCLUSION

Enclosed is a check for $110.00 for a one month extension of time. The Commissioner is hereby authorized to charge any underpayment and credit any overpayment of government fees to Deposit Account No. 19-1345.

Respectfully submitted,



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